CS 194 – Introduction to Digital Design

General Description: CS 194 – Introduction to Digital Design (with Lab, 4 credit hours)
It is very important for all engineering students, specifically for the students in Electrical
Engineering and Computer Science fields, to understand logic design concepts. The objective of
this course is to teach the fundamental concepts of digital design, including number systems,
Boolean algebra, Karnaugh maps, combinational circuit design, adders, decoders, multiplexers,
sequential circuit design, state diagram, flip flops, and sequence detectors. In addition, techniques
to test different combinational and sequential circuits should be discussed in brief. Laboratory
assignments should help students apply their classroom knowledge and gain hands-on experience.

The pre-requisite for this course is MATH 111 (or equivalent). By continued enrollment in this class, you
are certifying that you have met the pre-requisite.

Instructor: Abu Asaduzzaman
Office: Jabara Hall #253
Office Hours: Wednesdays…9:30 am – 12:00 noon
Thursdays……9:30 am – 11:15 am
Or, by appointment (e-mail/phone)
E-mail: Abu.Asaduzzaman@wichita.edu
Phone: 316-978-5261 (Office); 561-843-2231 (Mobile)

Text-Book: Introduction to Logic Design (3rd Ed.) by Alan B. Marcovitz

Topics Include:
Chapter 1: Introduction
   a) Number Systems (Binary, Decimal, Hexadecimal, and others)
   b) Signed Numbers
   c) Binary Addition, Subtraction
Chapter 2: Combinational Circuits
   a) Switching Algebra and Logic Gates (AND, OR, and NOT)
   b) Truth Table Analysis of Combinational Circuits
   c) The Complement and Don’t Care Conditions
   d) Universal Gates (NAND and NOR realizations of all gates)
Chapter 3: The Karnaugh Map
   a) The Karnaugh Map (K-map) and its applications
   b) Minimum Sum of Products Expressions Using the K-map
   c) Minimum Product of Sums Solutions Using the K-map
Chapter 5: Designing Combinational Systems
   a) Combinational Logic Circuit Design and Analysis
   b) Adders/Subtractors, Comparators
   c) Decoders/Encoders
   d) Multiplexers/Demultiplexers
   e) Gate Arrays (ROMs, PLAs, and PALs)
   f) Displays (e.g., Driver for Seven-Segment Display)
Chapters 6, 7, and 8: Analysis and Design of Sequential Systems
   a) State Tables, State Diagrams, Timing Diagrams
   b) Latches, Delay, Set-Reset, Toggle, and J-K Flip Flops
   c) Shift Registers and Counters
Grading Policy:
(Tentative)
Exams (best 3 out of 4): (22 x 3) = 66%
Homework: (2, 2, 2, 3, 3) = 14%
Laboratory Work: (10 x 2) = 20%

Your final course grade will be approximately based on the following:
A: 93  A−: 90  B+: 87  B: 83  B−: 80  C+: 77  C: 73  C−: 70  D+: 67  D: 63  D−: 60  F: 0

Exam Schedule:
(Tentative)
Exam 1: Sep. 21 (Tuesday) in class
Exam 2: Oct. 19 (Tuesday) in class
Exam 3: Nov. 16 (Tuesday) in class
Exam 4 (Optional): Dec. 9 (Thursday) in class

Other Policies:
1. Homework is due at the beginning of the class of the due dates. Late homework will not be accepted without prior consent.
2. Everyone must turn in his or her own homework, unless permission is given.
3. Make-up exams will only be given in the event of an emergency or with prior consent. If the reason for missing an exam is illness, a doctor’s note will be consent.
4. All academic dishonesty cases will be handled following the University Code of Academic Conduct. You may check the University Catalog for further information.

Laboratory Information:
Sections: CS 194L 15315 → Tue 11:30 am – 1:20 pm; WH 330
        CS 194L 15783 → Thu 11:30 am – 1:20 pm; WH 330

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